Amendments to the Specification

Please amend the paragraph under the section of "Related Patent Application" on page 1 as follows:

Related U.S. patent application Ser. No. 10/855,086, ~~(MEG02-014),~~ to Water level processing method and structure to manufacture two kinds of bumps, gold and solder, on one wafer, ~~,~~ filed on May 27, 2004. ~~.~~

Please amend the paragraph bridging pages 2 and 3 as follows:

U.S. Patents 6,303,423 and 6,515,369, both by M.S. Lin, teach methods and structures of mounting a discrete component on the surface of an IC chip. Related Patent Application serial number ~~10/855,086~~ (MEG02-014) discloses methods of making both solder bumps and wirebond pads on the same wafer. U.S. Patents 6,495,442 and 6,383,916 to M.S. Lin et al disclose a post-passivation interconnection process. U.S. Patents 6,184,574 and 6,504,236 both to Bissey disclose an integrated circuit lead frame with capacitors formed on the lead frame and bonded to the bottom surface of the chip for decoupling purposes.

Please amend the first paragraph on page 7 as follows:

Referring now to FIG. 1, there is shown an example of a preferred embodiment of the present invention. Semiconductor substrate 10 is shown. Transistors and other devices, not shown, are formed in and on the semiconductor substrate 10. Dielectric layer 12 is formed over the substrate 10. Conductive interconnect lines 11 are formed within the dielectric layer connecting to devices formed in and on the substrate, not shown. Layers 14 represent the plurality of metal and dielectric layers formed in a typical integrated circuit. Two layers 14 are shown in FIG. 1, including metal interconnects 13. Multiple layers of dielectric materials may be included in layers 14. More than two layers 14 may be present. Overlying these layers 14 are points of contact 16 that will be connected to surrounding circuitry. Passivation layer 18 is formed over the contacts 16. The contacts 16 may be an aluminum pad. The passivation layer may comprise silicon oxide or silicon nitride or a composite of these materials. The passivation layer prevents the penetration of mobile ions, such as sodium ions, moisture, transition metals, such as gold, silver, copper, and so on, and other contaminations. The passivation layer is used to protect the underlying devices, such as transistors, polysilicon resistors, poly-to-poly capacitors, and fine-line metal interconnections. Now, connection is to be made to the next level of packaging. Wirebonding is to be used in the connection. Discrete decoupling capacitors are mounted on the surface of the IC chip. In one preferred embodiment of the invention, the decoupling capacitors are connected to the wirebond through IC metal lines under the passivation layer. Discrete capacitors provide optimized parameters and can be mounted close to the circuits, which offer system-on-chip performance and minimizes parasitics. The post-passivation process of the present invention allows for the selection of discrete capacitor design parameters that result in reduced resistance of the discrete capacitor.

Please amend the second paragraph on page 9 as follows:

Solder ~~pads~~ 31 is ~~are~~ formed to connect the capacitor electrodes 34 to the metal segments Vdd and Vss. The capacitor 38 serves as a local power reservoir to decouple the external power ground noise caused by the wirebonds 26 and 28 and other system components. A decoupling capacitor is connected in association with each of at least two wirebonds.

Please amend the second paragraph on page 12 as follows:

In FIG. 5, for example, gold pads 40 are formed through openings in the passivation layer 18 to the metal lines 16 under the passivation layer. The gold pads 40 may be on the aluminum pad 16 exposed by an opening in the passivation layer 18. The wirebonds 26 and 28 are connected to the gold pads.